Sub-Contractors working with Fairbanks Laboratories, Inc.

Eng. 1: Layout Designer with over 12 years of experience in mask design using Cadence Virtuoso and Mentor IC Station for Hynix, XFAB, TSMC, AMI C5 wafer fabrication processes. Custom designs for digital and analog circuits. Verification tools supporting DRC & LVS.

Eng. 2: Analog IC Design Engineer with over 25 years of transistor-level integrated circuit experience, encompassing both bipolar and CMOS technologies. I have worked with high-speed and RF applications, as well as very low-power RFID applications. In my EE career I have worked in all phases of IC development, from design and simulation (Cadence, Mentor, HSPICE), to physical layout and verification (Diva, Calibre), to back-end analysis and characterization.

Eng. 3: RF/analog design engineer with MSEE and over 10 years experience using IBM processes for VCO, PA, and other analog blocks. Design using Cadence to 45 nm. Board design using Altium to support testing of receive and transmit circuits, including automation of test using LabView.

Eng. 4: An RF Engineer with over 25 years experience specializing in EM, RF Circuit, and Digital Signal Integrity applications utilizing the latest simulation software for fast and accurate designs. Has worked through several designs using HFSS, CST, & EM Pro. Has simulated systems using ADS and testing using LabView.

Eng. 5: Full custom analog/mixed signal/rfic IC design engineer with 35 years experience creating the following: high Speed LVDS Transceivers, DC-DC power converters, high speed LVDS transceivers, DC-DC power converters, digitally trimmable temperature sensor circuits, low power voltage regulators, bandgap voltage references, temperature sensors, crystal oscillators, and RFID demodulator circuits. Experienced and proficient in Mentor and Cadence IC design systems.

