## Test Methodology

FairLabs has built several custom design verification systems for industry and academia. These involved testing transistors and other test structures, under varying conditions. Wafer level testing, including devices and circuits, as well as multi-function chips at the package level have been tested using systems designed and developed by FairLabs. Each of these systems were automated under computer control. Performance reports which extended from device characteristics to models to circuit performance to system functions were produced using modeling software under computer control.

Wafer: Keithley Parametric Test system for wafer fabrication monitoring at two different foundries
Focus Load-pull Test system for receiver power, intermodulation, and noise measurements, frequently used for PA's as well. Can also be used at board level.

IC: Using custom high frequency matrix and instruments, via custom boards for receiver IC functions.

Module: LTCC studies for Satellite TR switch.

Tags: Digital and RF testing of assembled RFID's.